ABSTRACT OF THE DISCLOSURE

A vertical MOS transistor has an epitaxial growth layer disposed on a semiconductor substrate, a body region disposed on the epitaxial growth layer, a heavily doped body contact region disposed on a part of the body region, a heavily doped source region disposed on a part of the body region on which the body contact region is not disposed, and a silicon trench extending through the source region and the body region and extending into the epitaxial growth layer. A gate insulating film is disposed on sidewall and bottom surfaces of the silicon trench. A heavily doped polycrystalline silicon gate is disposed in the silicon trench over the gate insulating film and extends below a surface formed by the body region and the body contact region. An intermediate insulating film is disposed on the polycrystalline silicon gate in the silicon trench so as to reach the surface formed by the body region and the body contact region. An insulator is disposed on the sidewalls of the silicon trench and above the polycrystalline silicon gate.